Applicant : Yusuke Igarashi et al.
 Attorney's Docket No.: 14225

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 111US1/F1040900US00

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Amendments to the Specification:

Please replace the paragraph beginning at page 9, line 16 with the following amended paragraphs:

-- The conductive patterns 18 are made of metal such as copper and formed so as to be insulated from the eireuit substrate 16. Moreover, pads composing of the conductive patterns 18 are formed along a side from which leads 11 extend. Although the description is given of a case where the leads extend from one side, it is sufficient that the leads extend from at least one side. Moreover, the conductive patterns 18 are bonded to the surface of the circuit substrate 16 by using the insulating layer 17 as an adhesive. The conductive patterns 18 include the first conductive pattern 18A and the second conductive pattern 18B formed more thickly than the first conductive pattern 18A. Additionally, the first conductive pattern 18B. --

Please replace the paragraph beginning at page 11, line 8 with the following amended paragraphs:

Referring to the perspective view of Fig. 2, examples of specific shapes of the conductive patterns 18 formed on the surface of the circuit substrate 16 will be described. In this drawing, the resin for sealing the entire device is omitted.--

Please replace the paragraph beginning at page 11, line 20 with the following amended paragraphs:

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-- Here, a pattern connected to the first circuit element 144A which is an LSI element is constituted of the first conductive pattern 18A. Since an electric signal used in a signal processing of an LSI element is approximately several milliamperes, the current-carrying capacitance of the first conductive pattern 18A having a thickness of approximately several tens of micrometers is sufficient. In addition, since the first conductive pattern 18A is finely formed, an LSI element having a large number of terminals can also be employed as the first circuit element 14A.--

Please replace the paragraph beginning at page 14, line 24 with the following amended paragraphs:

 Next, referring to Figs. 4A to 4F and subsequent drawings, a method of manufacturing the above-described hybrid integrated circuit device will be described.--

Please replace the paragraph beginning at page 16 through 17, line 6 with the following amended paragraphs:

The edge portion 18D is formed so as to two-dimensionally surround the protruding portion 22. In other words, the edge portion 18D is formed by forming the resist 21, which covers the upper portion of the protruding portion 22, to be larger than the protruding portion 22. Thus, when the second conductive pattern 18B is etched, a stable etching can be performed by forming the resist 21 to be larger. That is, since the wet etching is isotropic, side etching proceeds on the conductive patterns 18, and patterned side surfaces of the second conductive pattern 18B have tapered shapes.

Accordingly, by performing the etching largely as described above, the second conductive pattern 18[B] can be prevented from being eroded by the side etching.—

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Please replace the paragraph beginning at page 17, line 24 with the following amended paragraphs:

-- First, referring to Figs. 5A to 5C, a conductive foil 20 is brought into intimate contact with an insulating layer 17 applied on a surface of a circuit substrate 16. Here, the conductive foil 20 is bounded by pressure bonding is performed while maintaining the thickness. Thereby, it is possible to suppress occurrence of "a wrinkle" of the conductive foil 20 in the pressure bonding step. After a region in which the thick second conductive pattern 18[[B]] is to be formed is covered with a resist 21, the surface of the conductive foil 20 is etched. By this etching, the conductive foil 20 in the region in which a thin first conductive pattern 18A is to be formed is made sufficiently thin. After this etching is finished, the resist 21 is removed.--

Please replace the paragraph beginning at page 19 through 20, line 2 with the following amended paragraphs:

-- First, referring to Fig. 8A, circuit elements 14 are fixed to conductive patterns (islands) 18 with solder, conductive paste or the like. Here, a first circuit element 14A which processes a small current is fixed to a first conductive pattern 18A. On the other hand, a second circuit element 14B, through which a large current flows, and which generates a large amount of heat, is fixed to a second conductive pattern 18B. Since a fine pattern can be realized in the first conductive pattern 18A, an element having a large number of terminals, such as an LSI, can be employed as the first circuit element 14A. Since the second conductive pattern 18B is formed to be thick sufficiently, a power transistor, an LSI or the like, which processes a large current, can be employed as the second circuit element 18 [[14]]B. Here, a plurality of units 24 constituting one hybrid

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integrated circuit device are formed on one piece of a circuit substrate 16, and die bonding thereof and wire bonding thereof can be collectively performed.--

Please replace the paragraph beginning at page 20, line 9 with the following amended paragraphs:

-- Referring to Fig. 8B, each of the circuit elements 14 and each of the conductive patterns 18 are electrically connected to each other through thin metal wires 15. In this embodiment, since a thick portion of the second conductive pattern 18B is buried in an insulating layer resin 17, the upper surfaces of the first and second conductive patterns 18A and 18B are on the same level. Accordingly, it becomes possible to use thin wires of approximately several tens of micrometers for an electrical connection of the second circuit element 14B. Conventionally, a deference of elevation has been large between a transistor mounted on an upper portion of a heat sink or the like and the conductive patterns 18. In some case, this difference of elevation is, for example, approximately 2 mm. Accordingly, firm thick wires have been used in order to prevent the wires from drooping due to their own weights and from causing a ship or a heat sink to short out. In this embodiment, since the upper surface of the second conductive pattern 18B corresponding to a heat sink is on a level equal to that of the first conductive pattern 18A, there is no need to use the firm thick wires. Here, the thin wires generally mean thin metal wires having diameters of approximately 80 μm.—

Please replace the paragraph beginning at page 21, line 6 with the following amended paragraphs:

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In the conventional hybrid integrated circuit substrates, all conductive patterns have been formed to have the same film thickness. Accordingly, in a portion through which a large current is required to flow, a pattern having a large width has been formed, or a heat sink has been additionally employed. However, in this application, a thick second eenductive pattern 18B and a thin first pattern 18A can be formed on the same hybrid integrated circuit substrate. Accordingly, heat dissipation and a current-carrying capacitance are ensured by the thick second conductive pattern 18B. In addition, providing the thin first conductive pattern 18A makes it possible to mount a small-signal component.—

Please replace the paragraph beginning at page 21, line 14 with the following amended paragraphs:

-- For example, in a case where a circuit substrate 16 made of Al is used, heat dissipation can be improved by burying a protruding portion 22, which is formed in the second conductive pattern 18B, in an insulating layer 17 covering the surface of the eireuit substrate 16. This is because heat generated in a circuit element fixed to the second conductive pattern 18B is suitably conducted to the circuit substrate 16 through the protruding portion 22 buried in the insulating layer 17. If a filler is mixed in the insulating layer 17, the heat dissipation is further improved.--